METHOD FOR MAKING SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE

Related Applications

[0001]   This application is a continuation-in-part of U.S. Patent Applications Serial Nos. _____ and _____ filed on June 26, 2003, entitled "Semiconductor Structures Having Improved Conductivity Effective Mass" attorney work docket 0002-0001, and "Methods of Fabricating Semiconductor Structures Having Improved Conductivity Effective Mass" attorney work docket no. 0002-0002, the entire disclosures of which are incorporated by reference herein.

Field of the Invention

[0002]   The present invention relates to the field of semiconductors, and, more particularly, to semiconductors having enhanced properties based upon energy band engineering and associated methods.

Background of the Invention

[0003]   Structures and techniques have been proposed to enhance the performance of semiconductor devices, such as

by enhancing the mobility of the charge carriers. For example, U.S. Patent Application No. 2003/0057416 to Currie et al. discloses strained material layers of silicon, silicon-germanium, and relaxed silicon and also including impurity-free zones that would otherwise cause performance degradation. The resulting biaxial strain in the upper silicon layer alters the carrier mobilities enabling higher speed and/or lower power devices. Published U.S. Patent Application No. 2003/0034529 to Fitzgerald et al. discloses a CMOS inverter also based upon similar strained silicon technology.

[0004] U.S. Patent No. 6,472,685 B2 to Takagi discloses a semiconductor device including a silicon and carbon layer sandwiched between silicon layers so that the conduction band and valence band of the second silicon layer receive a tensile strain. Electrons having a smaller effective mass, and which have been induced by an electric field applied to the gate electrode, are confined in the second silicon layer, thus, an n-channel MOSFET is asserted to have a higher mobility.

[0005] U.S. Patent No. 4,937,204 to Ishibashi et al. discloses a superlattice in which a plurality of layers, less than eight monolayers, and containing a fraction or a binary compound semiconductor layers, are alternately and epitaxially grown. The direction of main current flow is perpendicular to the layers of the superlattice.

[0006] U.S. Patent No. 5,357,119 to Wang et al. discloses a Si-Ge short period superlattice with higher mobility achieved by reducing alloy scattering in the superlattice. Along these lines, U.S. Patent No. 5,683,934 to Candelaria discloses an enhanced mobility MOSFET including a channel layer comprising an alloy of silicon

and a second material substitutionally present in the silicon lattice at a percentage that places the channel layer under tensile stress.

[0007]   U.S. Patent No. 5,216,262 to Tsu discloses a quantum well structure comprising two barrier regions and a thin epitaxially grown semiconductor layer sandwiched between the barriers. Each barrier region consists of alternate layers of SiO_2/Si with a thickness generally in a range of two to six monolayers. A much thicker section of silicon is sandwiched between the barriers.

[0008]   An article entitled "Phenomena in silicon nanostructure devices" also to Tsu and published online September 6, 2000 by Applied Physics and Materials Science & Processing, pp. 391-402 discloses a semiconductor-atomic superlattice (SAS) of silicon and oxygen. The Si/O superlattice is disclosed as useful in a silicon quantum and light-emitting devices. In particular, a green electromuminescence diode structure was constructed and tested. Current flow in the diode structure is vertical, that is, perpendicular to the layers of the SAS. The disclosed SAS may include semiconductor layers separated by adsorbed species such as oxygen atoms, and CO molecules. The silicon growth beyond the adsorbed monolayer of oxygen is described as epitaxial with a fairly low defect density. One SAS structure included a 1.1 nm thick silicon portion that is about eight atomic layers of silicon, and another structure had twice this thickness of silicon. An article to Luo et al. entitled "Chemical Design of Direct-Gap Light-Emitting Silicon" published in Physical Review Letters, Vol. 89, No. 7 (August 12, 2002) further discusses the light emitting SAS structures of Tsu.

[0009]   Published International Application WO 02/103,767 A1 to Wang, Tsu and Lofgren, discloses a barrier building block of thin silicon and oxygen, carbon, nitrogen, phosphorous, antimony, arsenic or hydrogen to thereby reduce current flowing vertically through the lattice more than four orders of magnitude. The insulating layer/barrier layer allows for low defect epitaxial silicon to be deposited next to the insulating layer.

[0010]   Published Great Britain Patent Application 2,347,520 to Mears et al. discloses that principles of Aperiodic Photonic Band-Gap (APBG) structures may be adapted for electronic bandgap engineering. In particular, the application discloses that material parameters, for example, the location of band minima, effective mass, etc, can be tailored to yield new aperiodic materials with desirable band-structure characteristics. Other parameters, such as electrical conductivity, thermal conductivity and dielectric permittivity or magnetic permeability are disclosed as also possible to be designed into the material.

[0011]   Despite considerable efforts at materials engineering to increase the mobility of charge carriers in semiconductor devices, there is still a need for greater improvements. Greater mobility may increase device speed and/or reduce device power consumption. With greater mobility, device performance can also be maintained despite the continued shift to smaller device features.

Summary of the Invention

[0012]   In view of the foregoing background, it is therefore an object of the present invention to provide a

method for making a semiconductor device having a higher charge carrier mobility, for example.

[0013]   This and other objects, features and advantages in accordance with the invention are provided by a method including forming a superlattice including a plurality of stacked groups of layers, and forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers. Each group of layers of the superlattice may comprise a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon. Moreover, the energy-band modifying layer may comprise at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice and has a higher charge carrier mobility in the parallel direction than would otherwise be present. The superlattice may also have a common energy band structure therein.

[0014]   The charge carriers may comprise at least one of electrons and holes. In some preferred embodiments, each base semiconductor portion may comprise silicon, and each energy band-modifying layer may comprise oxygen. Each energy band-modifying layer may be a single monolayer thick, and each base semiconductor portion may be less than eight monolayers thick, such as two to four layers thick, for example, in some embodiments.

[0015]   As a result of the band engineering achieved by the present invention, the superlattice may further have a substantially direct energy bandgap. The superlattice may further comprise a base semiconductor cap layer on an uppermost group of layers.

[0016]   In some embodiments, all of the base
semiconductor portions may be a same number of monolayers
thick.   In other embodiments, at least some of the base
semiconductor portions may be a different number of
monolayers thick.   In still other embodiments, all of the
base semiconductor portions may be a different number of
monolayers thick.

[0017]   Each non-semiconductor monolayer is desirably
thermally stable through deposition of a next layer to
thereby facilitate manufacturing.   Each base semiconductor
portion may comprise a base semiconductor selected from the
group consisting of Group IV semiconductors, Group III-V
semiconductors, and Group II-VI semiconductors.   In
addition, each energy band-modifying layer may comprise a
non-semiconductor selected from the group consisting of
oxygen, nitrogen, fluorine, and carbon-oxygen.

[0018]   The higher charge carrier mobility may result
from a lower conductivity effective mass for the charge
carriers in the parallel direction than would otherwise be
present.   The conductivity effective mass may be less than
two-thirds the conductivity effective mass that would
otherwise occur.   Of course, the superlattice may further
comprise at least one type of conductivity dopant therein.

Brief Description of the Drawings

[0019]   FIG. 1 is a schematic cross-sectional view of a
semiconductor device in accordance with the present
invention.

[0020]   FIG. 2 is a greatly enlarged schematic cross-
sectional view of the superlattice as shown in FIG. 1.

[0021]   FIG. 3 is a perspective schematic atomic diagram
of a portion of the superlattice shown in FIG. 1.

[0022]   FIG. 4 is a greatly enlarged schematic cross-sectional view of another embodiment of a superlattice that may be used in the device of FIG. 1.

[0023]   FIG. 5A is a graph of the calculated band structure from the gamma point (G) for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. 1-3.

[0024]   FIG. 5B is a graph of the calculated band structure from the Z point for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. 1-3.

[0025]   FIG. 5C is a graph of the calculated band structure from both the gamma and Z points for both bulk silicon as in the prior art, and for the 5/1/3/1 Si/O superlattice as shown in FIG. 4.

[0026]   FIGS. 6A-6H are schematic cross-sectional views of a portion of another semiconductor device in accordance with the present invention during the making thereof.

Detailed Description of the Preferred Embodiments

[0027]   The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout and prime notation is used to indicate similar elements in alternate embodiments.

[0028]   The present invention relates to controlling the properties of semiconductor materials at the atomic or molecular level to achieve improved performance within semiconductor devices.   Further, the invention relates to the identification, creation, and use of improved materials for use in the conduction paths of semiconductor devices.

[0029]   Applicants theorize, without wishing to be bound thereto, that certain superlattices as described herein reduce the effective mass of charge carriers and that this thereby leads to higher charge carrier mobility. Effective mass is described with various definitions in the literature. As a measure of the improvement in effective mass Applicants use a "conductivity reciprocal effective mass tensor", M_e^{-1} and M_h^{-1} for electrons and holes respectively, defined as:

$$\mathbf{M}_{e,ij}^{-1}(E_F,T) = \frac{\sum_{E>E_F} \int_{B.Z.} (\nabla_{\mathbf{k}}E(\mathbf{k},n))_i \, (\nabla_{\mathbf{k}}E(\mathbf{k},n))_j \, \frac{\partial f(E(\mathbf{k},n),E_F,T)}{\partial E} d^3\mathbf{k}}{\sum_{E>E_F} \int_{B.Z.} f(E(\mathbf{k},n),E_F,T) d^3\mathbf{k}}$$

for electrons and:

$$\mathbf{M}_{h,ij}^{-1}(E_F,T) = \frac{-\sum_{E<E_F} \int_{B.Z.} (\nabla_{\mathbf{k}}E(\mathbf{k},n))_i \, (\nabla_{\mathbf{k}}E(\mathbf{k},n))_j \, \frac{\partial f(E(\mathbf{k},n),E_F,T)}{\partial E} d^3\mathbf{k}}{\sum_{E<E_F} \int_{B.Z.} (1 - f(E(\mathbf{k},n),E_F,T)) d^3\mathbf{k}}$$

for holes, where f is the Fermi-Dirac distribution, E_F is the Fermi energy, T is the temperature, E(k,n) is the energy of an electron in the state corresponding to wave vector k and the nth energy band, the indices i and j refer to cartesian coordinates x, y and z, the integrals are

taken over the Brillouin zone (B.Z.), and the summations are taken over bands with energies above and below the Fermi energy for electrons and holes respectively.

[0030]   Applicants' definition of the conductivity reciprocal effective mass tensor is such that a tensorial component of the conductivity of the material is greater for greater values of the corresponding component of the conductivity reciprocal effective mass tensor.   Again Applicants theorize without wishing to be bound thereto that the superlattices described herein set the values of the conductivity reciprocal effective mass tensor so as to enhance the conductive properties of the material, such as typically for a preferred direction of charge carrier transport. The inverse of the appropriate tensor element is referred to as the conductivity effective mass.   In other words, to characterize semiconductor material structures, the conductivity effective mass for electrons/holes as described above and calculated in the direction of intended carrier transport is used to distinguish improved materials.

[0031]   Using the above-described measures, one can select materials having improved band structures for specific purposes.   One such example would be a superlattice **25** material for a channel region in a CMOS device.   A planar MOSFET **20** including the superlattice **25** in accordance with the invention is now first described with reference to FIG. 1.   One skilled in the art, however, will appreciate that the materials identified herein could be used in many different types of semiconductor devices, such as discrete devices and/or integrated circuits.

[0032]   The illustrated MOSFET **20** includes a substrate **21**, source/drain regions **22**, **23**, source/drain extensions

26, 27, and a channel region therebetween provided by the superlattice **25**. Source/drain silicide layers **30, 31** and source/drain contacts **32, 33** overlie the source/drain regions as will be appreciated by those skilled in the art. Regions indicated by dashed lines **34, 35** are optional vestigial portions formed originally with the superlattice, but thereafter heavily doped. In other embodiments, these vestigial superlattice regions **34, 35** may not be present as will also be appreciated by those skilled in the art. A gate **35** illustratively includes a gate insulating layer **37** adjacent the channel provided by the superlattice **25**, and a gate electrode layer **36** on the gate insulating layer. Sidewall spacers **40, 41** are also provided in the illustrated MOSFET **20**.

[0033] Applicants have identified improved materials or structures for the channel region of the MOSFET **20**. More specifically, the Applicants have identified materials or structures having energy band structures for which the appropriate conductivity effective masses for electrons and/or holes are substantially less than the corresponding values for silicon.

[0034] Referring now additionally to FIGS. 2 and 3, the materials or structures are in the form of a superlattice **25** whose structure is controlled at the atomic or molecular level and may be formed using known techniques of atomic or molecular layer deposition. The superlattice **25** includes a plurality of layer groups **45a-45n** arranged in stacked relation as perhaps best understood with specific reference to the schematic cross-sectional view of FIG. 2.

[0035] Each group of layers **45a-45n** of the superlattice **25** illustratively includes a plurality of stacked base semiconductor monolayers **46** defining a respective base

semiconductor portion **46a-46n** and an energy band-modifying layer **50** thereon. The energy band-modifying layers **50** are indicated by stippling in FIG. 2 for clarity of explanation.

[0036]   The energy-band modifying layer **50** illustratively comprises one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. In other embodiments, more than one such monolayer may be possible. Applicants theorize without wishing to be bound thereto that energy band-modifying layers **50** and adjacent base semiconductor portions **46a-46n** cause the superlattice **25** to have a lower appropriate conductivity effective mass for the charge carriers in the parallel layer direction than would otherwise be present. Considered another way, this parallel direction is orthogonal to the stacking direction. The band modifying layers **50** may also cause the superlattice **25** to have a common energy band structure. It is also theorized that the semiconductor device, such as the illustrated MOSFET **20**, enjoys a higher charge carrier mobility based upon the lower conductivity effective mass than would otherwise be present. In some embodiments, and as a result of the band engineering achieved by the present invention, the superlattice **25** may further have a substantially direct energy bandgap that may be particularly advantageous for opto-electronic devices, for example, as described in further detail below.

[0037]   As will be appreciated by those skilled in the art, the source/drain regions **22, 23** and gate **35** of the MOSFET **20** may be considered as regions for causing the transport of charge carriers through the superlattice in a parallel direction relative to the layers of the stacked

groups **45a-45n**. Other such regions are also contemplated by the present invention.

[0038]   The superlattice **25** also illustratively includes a cap layer **52** on an upper layer group **45n**. The cap layer **52** may comprise a plurality of base semiconductor monolayers **46**. The cap layer **52** may have between 2 to 100 monolayers of the base semiconductor, and, more preferably between 10 to 50 monolayers.

[0039]   Each base semiconductor portion **46a-46n** may comprise a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors. Of course, the term Group IV semiconductors also includes Group IV-IV semiconductors as will be appreciated by those skilled in the art.

[0040]   Each energy band-modifying layer **50** may comprise a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen, for example. The non-semiconductor is also desirably thermally stable through deposition of a next layer to thereby facilitate manufacturing. In other embodiments, the non-semiconductor may be another inorganic or organic element or compound that is compatible with the given semiconductor processing as will be appreciated by those skilled in the art.

[0041]   It should be noted that the term monolayer is meant to include a single atomic layer and also a single molecular layer. It is also noted that the energy band-modifying layer **50** provided by a single monolayer is also meant to include a monolayer wherein not all of the possible sites are occupied. For example, with particular reference to the atomic diagram of FIG. 3, a 4/1 repeating structure is illustrated for silicon as the base

semiconductor material, and oxygen as the energy band-modifying material. Only half of the possible sites for oxygen are occupied. In other embodiments and/or with different materials this one half occupation would not necessarily be the case as will be appreciated by those skilled in the art. Indeed it can be seen even in this schematic diagram, that individual atoms of oxygen in a given monolayer are not precisely aligned along a flat plane as will also be appreciated by those of skill in the art of atomic deposition.

[0042] Silicon and oxygen are currently widely used in conventional semiconductor processing, and, hence, manufacturers will be readily able to use these materials as described herein. Atomic or monolayer deposition is also now widely used. Accordingly, semiconductor devices incorporating the superlattice **25** in accordance with the invention may be readily adopted and implemented as will be appreciated by those skilled in the art.

[0043] It is theorized without Applicants wishing to be bound thereto, that for a superlattice, such as the Si/O superlattice, for example, that the number of silicon monolayers should desirably be seven or less so that the energy band of the superlattice is common or relatively uniform throughout to achieve the desired advantages. The 4/1 repeating structure shown in FIGS. 2 and 3, for Si/O has been modeled to indicate an enhanced mobility for electrons and holes in the X direction. For example, the calculated conductivity effective mass for electrons (isotropic for bulk silicon) is 0.26 and for the 4/1 SiO superlattice in the X direction it is 0.12 resulting in a ratio of 0.46. Similarly, the calculation for holes yields

values of 0.36 for bulk silicon and 0.16 for the 4/1 Si/O superlattice resulting in a ratio of 0.44.

[0044]   While such a directionally preferential feature may be desired in certain semiconductor devices, other devices may benefit from a more uniform increase in mobility in any direction parallel to the groups of layers. It may also be beneficial to have an increased mobility for both electrons or holes, or just one of these types of charge carriers as will be appreciated by those skilled in the art.

[0045]   The lower conductivity effective mass for the 4/1 Si/O embodiment of the superlattice **25** may be less than two-thirds the conductivity effective mass than would otherwise occur, and this applies for both electrons and holes. Of course, the superlattice **25** may further comprise at least one type of conductivity dopant therein as will also be appreciated by those skilled in the art.

[0046]   Indeed, referring now additionally to FIG. 4 another embodiment of a superlattice **25'** in accordance with the invention having different properties is now described. In this embodiment, a repeating pattern of 3/1/5/1 is illustrated. More particularly, the lowest base semiconductor portion **46a'** has three monolayers, and the second lowest base semiconductor portion **46b'** has five monolayers. This pattern repeats throughout the superlattice **25'** The energy band-modifying layers **50'** may each include a single monolayer. For such a superlattice **25'** including Si/O, the enhancement of charge carrier mobility is independent of orientation in the plane of the layers. Those other elements of FIG. 4 not specifically mentioned are similar to those discussed above with reference to FIG. 2 and need no further discussion herein.

[0047]   In some device embodiments, all of the base
semiconductor portions of a superlattice may be a same
number of monolayers thick.   In other embodiments, at least
some of the base semiconductor portions may be a different
number of monolayers thick.   In still other embodiments,
all of the base semiconductor portions may be a different
number of monolayers thick.

[0048]   In FIGS. 5A-5C band structures calculated using
Density Functional Theory (DFT) are presented.   It is well
known in the art that DFT underestimates the absolute value
of the bandgap.   Hence all bands above the gap may be
shifted by an appropriate "scissors correction".   However
the shape of the band is known to be much more reliable.
The vertical energy axes should be interpreted in this
light.

[0049]   FIG. 5A shows the calculated band structure from
the gamma point (G) for both bulk silicon (represented by
continuous lines) and for the 4/1 Si/O superlattice 25 as
shown in FIGS. 1-3 (represented by dotted lines). The
directions refer to the unit cell of the 4/1 Si/O structure
and not to the conventional unit cell of Si, although the
(001) direction in the figure does correspond to the (001)
direction of the conventional unit cell of Si, and, hence,
shows the expected location of the Si conduction band
minimum. The (100) and (010) directions in the figure
correspond to the (110) and (-110) directions of the
conventional Si unit cell. Those skilled in the art will
appreciate that the bands of Si on the figure are folded to
represent them on the appropriate reciprocal lattice
directions for the 4/1 Si/O structure.

[0050]   It can be seen that the conduction band minimum
for the 4/1 Si/O structure is located at the gamma point in

contrast to bulk silicon (Si), whereas the valence band minimum occurs at the edge of the Brillouin zone in the (001) direction which we refer to as the Z point. One may also note the greater curvature of the conduction band minimum for the 4/1 Si/O structure compared to the curvature of the conduction band minimum for Si owing to the band splitting due to the perturbation introduced by the additional oxygen layer.

[0051] FIG. 5B shows the calculated band structure from the Z point for both bulk silicon (continuous lines) and for the 4/1 Si/O superlattice 25 (dotted lines). This figure illustrates the enhanced curvature of the valence band in the (100) direction.

[0052] FIG. 5C shows the calculated band structure from the both the gamma and Z point for both bulk silicon (continuous lines) and for the 5/1/3/1 Si/O structure of the superlattice 25' of FIG. 4 (dotted lines). Due to the symmetry of the 5/1/3/1 Si/O structure, the calculated band structures in the (100) and (010) directions are equivalent. Thus the conductivity effective mass and mobility are expected to be isotropic in the plane parallel to the layers, i.e. perpendicular to the (001) stacking direction. Note that in the 5/1/3/1 Si/O example the conduction band minimum and the valence band maximum are both at or close to the Z point. Although increased curvature is an indication of reduced effective mass, the appropriate comparison and discrimination may be made via the conductivity reciprocal effective mass tensor calculation. This leads Applicants to further theorize that the 5/1/3/1 superlattice 25' should be substantially direct bandgap. As will be understood by those skilled in the art, the appropriate matrix element for optical

transition is another indicator of the distinction between direct and indirect bandgap behavior.

[0053]   Referring now additionally to FIGS. 6A-6H, a discussion is provided of the formation of a channel region provided by the above-described superlattice **25** in a simplified CMOS fabrication process for manufacturing PMOS and NMOS transistors. The example process begins with an eight-inch wafer of lightly doped P-type or N-type single crystal silicon with <100> orientation **402**. In the example, the formation of two transistors, one NMOS and one PMOS will be shown. In FIG. 6A, a deep N-well **404** is implanted in the substrate **402** for isolation. In FIG. 6B, N-well and P-well regions **406, 408**, respectively, are formed using an SiO_2/Si_3N_4 mask prepared using known techniques. This could entail, for example, steps of n-well and p-well implantation, strip, drive-in, clean, and re-growth. The strip step refers to removing the mask (in this case, photoresist and silicon nitride). The drive-in step is used to locate the dopants at the appropriate depth, assuming the implantation is lower energy (i.e. 80keV) rather than higher energy (200-300keV). A typical drive-in condition would be approximately 9-10 hrs. at 1100-1150°C. The drive-in step also anneals out implantation damage. If the implant is of sufficient energy to put the ions at the correct depth then an anneal step follows, which is lower temperature and shorter. A clean step comes before an oxidation step so as to avoid contaminating the furnaces with organics, metals, etc. Other known ways or processes for reaching this point may be used as well.

[0054]   In FIGS. 6C-6H, an NMOS device will be shown in one side **200** and a PMOS device will be shown in the other side **400**. FIG. 6C depicts shallow trench isolation in which

the wafer is patterned, the trenches **410** are etched (0.3-0.8 um), a thin oxide is grown, the trenches are filled with SiO_2, and then the surface is planarized. FIG. 6D depicts the definition and deposition of the superlattice of the present invention as the channel regions **412, 414**. An SiO_2 mask (not shown) is formed, a superlattice of the present invention is deposited using atomic layer deposition, an epitaxial silicon cap layer is formed, and the surface is planarized to arrive at the structure of FIG. 6D.

[0055]   The epitaxial silicon cap layer may have a preferred thickness to prevent superlattice consumption during gate oxide growth, or any other subsequent oxidations, while at the same time reducing or minimizing the thickness of the silicon cap layer to reduce any parallel path of conduction with the superlattice. According to the well known relationship of consuming approximately 45% of the underlying silicon for a given oxide grown, the silicon cap layer may be greater than 45% of the grown gate oxide thickness plus a small incremental amount to account for manufacturing tolerances known to those skilled in the art. For the present example, and assuming growth of a 25 angstrom gate, one may use approximately 13-15 angstroms of silicon cap thickness.

[0056]   FIG. 6E depicts the devices after the gate oxide layers and the gates are formed. To form these layers, a thin gate oxide is deposited, and steps of poly deposition, patterning, and etching are performed. Poly deposition refers to low pressure chemical vapor deposition (LPCVD) of silicon onto an oxide (hence it forms a polycrystalline material). The step includes doping with P+ or As- to make it conducting and the layer is around 250 nm thick.

[0057]   This step depends on the exact process, so the 250 nm thickness is only an example. The pattern step is made up of spinning photoresist, baking it, exposing it to light (photolithography step), and developing the resist. Usually, the pattern is then transferred to another layer (oxide or nitride) which acts as an etch mask during the etch step. The etch step typically is a plasma etch (anisotropic, dry etch) that is material selective (e.g. etches silicon 10 times faster than oxide) and transfers the lithography pattern into the material of interest.

[0058]   In FIG. 6F, lowly doped source and drain regions **420, 422** are formed. These regions are formed using n-type and p-type LDD implantation, annealing, and cleaning. "LDD" refers to n-type lowly doped drain, or on the source side, p-type lowly doped source. This is a low energy/low dose implant that is the same ion type as the source/drain. An anneal step may be used after the LDD implantation, but depending on the specific process, it may be omitted. The clean step is a chemical etch to remove metals and organics prior to depositing an oxide layer.

[0059]   FIG. 6G shows the spacer formation and the source and drain implants. An SiO_2 mask is deposited and etched back. N-type and p-type ion implantation is used to form the source and drain regions **430, 432, 434,** and **436**. Then the structure is annealed and cleaned. FIG. 6H depicts the self-aligned silicides formation, also known as salicidation. The salicidation process includes metal deposition (e.g. Ti), nitrogen annealing, metal etching, and a second annealing. This, of course, is just one example of a process and device in which the present invention may be used, and those of skill in the art will understand its application and use in many other processes

and devices. In other processes and devices the structures
of the present invention may be formed on a portion of a
wafer or across substantially all of a wafer. In other
processes and devices the structures of the present
invention may be formed on a portion of a wafer or across
substantially all of a wafer.

[0060]   In accordance with another manufacturing process
in accordance with the invention, selective deposition is
not used. Instead, a blanket layer may be formed and a
masking step may be used to remove material between
devices, such as using the STI areas as an etch stop.
This may use a controlled deposition over a patterned
oxide/Si wafer. The use of an atomic layer deposition tool
may also not be needed in some embodiments. For example,
the monolayers may be formed using a CVD tool with process
conditions compatible with control of monolayers as will be
appreciated by those skilled in the art. Although
planarization is discussed above, it may not be needed in
some process embodiments. The superlattice structure may
also formed prior to formation of the STI regions to
thereby eliminate a masking step. Moreover, in yet other
variations, the superlattice structure could be formed
prior to formation of the wells, for example.

[0061]   Considered in different terms, the method in
accordance with the present invention may include forming a
superlattice **25** including a plurality of stacked groups of
layers **45a-45n**. The method may also include forming
regions for causing transport of charge carriers through
the superlattice in a parallel direction relative to the
stacked groups of layers. Each group of layers of the
superlattice may comprise a plurality of stacked base
semiconductor monolayers defining a base semiconductor

portion and an energy band-modifying layer thereon. As described herein, the energy-band modifying layer may comprise at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice has a common energy band structure therein, and has a higher charge carrier mobility than would otherwise be present.

[0062] Other aspects relating to the present invention are disclosed in copending patent applications entitled "SEMICONDUCTOR DEVICE INCLUDING MOSFET HAVING BAND-ENGINEERED SUPERLATTICE", and "SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE", filed concurrently herein, and having respective attorney work docket nos. 62602, and 62601, the entire disclosures of which are incorporated herein by reference. In addition, many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.